Claims

We claim:

1. A process of fabricating a termination region for a trench MIS device comprising:

providing a semiconductor wafer, said wafer comprising a first layer of a first conductivity type and a second layer of a second conductivity type overlying said first layer;

forming a first trench in said wafer, said first trench coinciding with a scribe line bordering a die of said wafer, a bottom of said first trench being located in said second layer;

introducing a dopant of said first conductivity type through a bottom of said first trench to form a region of said first conductivity type extending from said bottom of said first trench to said first layer;

forming an insulating layer in said first trench and over a surface of said layer of second conductivity type;

forming a termination metal layer over said insulating layer in said first trench and over said surface of said layer of second conductivity type;

etching an opening in said metal layer at a bottom of said first trench, said scribe line intersecting said opening; and

sawing said wafer at said scribe line.

2. The process of Claim 1 comprising a forming a second trench in an active area of said die while forming said first trench, a bottom of said second trench being located in said second layer.

3. The process of Claim 2 comprising introducing a dopant of said first conductivity type through a bottom of said second trench while introducing a dopant of said first conductivity type through a bottom of said first trench to form a drain-drift region of said first conductivity type extending from said bottom of said second trench to said first layer.

4. The process of Claim 3 comprising forming a source region of said first conductivity type adjacent said second trench and said surface of said second layer.

5. The process of Claim 4 comprising introducing a conductive material into said second trench to form a gate.

6. The process of Claim 5 wherein forming said insulating layer comprises depositing an insulating layer that overlies said gate and extends into said first trench.

7. The process of Claim 6 comprising forming a source metal layer over said surface of said second layer, said source metal layer being in electrical contact with said source region.

8. The process of Claim 7 wherein said source metal layer extends into said first trench but does not extend to said scribe line.

9. The process of Claim 8 wherein said source metal layer overlies a junction of said region of first conductivity type.

10. The process of Claim 7 comprising forming an opening in said insulating layer at a bottom of said first trench.

11. The process of Claim 10 comprising patterning said source metal layer so as to form an edge segment, said edge segment bordering said scribe line and being electrically isolated from a remaining portion of said source metal layer, said edge segment extending into said opening in said insulating layer to make electrical contact with said region of first conductivity type.

12. The process of Claim 11 comprising forming a heavily-doped region of said first conductivity type within said region of first conductivity type, said edge segment being in electrical contact with said heavily-doped region of first conductivity type.

13. A semiconductor die comprising a trench MIS device, said die comprising a first layer of a first conductivity type and a second layer of a second conductivity type overlying said first layer, said die comprising a termination region comprising:

a half-trench formed in said second layer adjacent an edge of said die;

a region of said first conductivity type extending from a bottom of said half-trench to said first layer;

an insulating layer extending from said bottom of said half-trench, up a wall of said half-trench and over a surface of said second layer; and

a source metal layer over said insulating layer, said source metal layer extending from a location within said half-trench and over a surface of said second layer, said source metal layer being in electrical contact with a source region of said MIS device, an edge of said source metal layer in said half-trench being laterally spaced from said edge of said die.

14. The die of Claim 13 further comprising:

a trench located in said second layer in an active region of said die;

a drain-drift region of said first conductivity type extending from a bottom of said trench to said first layer; and

a conductive gate in said trench,

wherein said insulating layer extends from a location above said trench and into said half-trench.

15. The die of Claim 14 wherein said source region is located adjacent said trench.

16. The die of Claim 13 comprising a metal edge segment located in said half-trench adjacent said edge of said die, said metal edge segment being electrically isolated from said source metal layer and being in electrical contact with said region of first conductivity type.

17. The die of Claim 13 wherein said metal edge segment is in electrical contact with said region of first conductivity type through an opening in said insulated layer at said bottom of said half-trench.

18. The die of Claim 17 comprising a heavily-doped region of said first conductivity type within said region of first conductivity type and in contact with said metal edge segment.

19. The die of Claim 13 wherein said second layer comprises an epitaxial layer of said second conductivity type.

20. The die of Claim 19 wherein said first layer comprises a substrate and an epitaxial layer of said first conductivity type overlying said substrate.